BACKGROUND ART

FIG. 1A

FIG. 1B

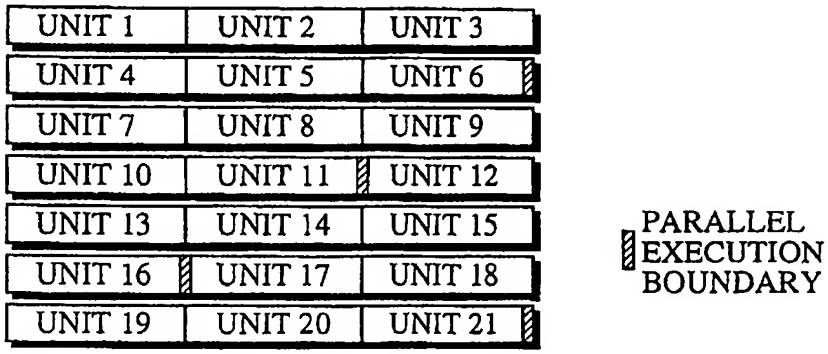


FIG. 1C

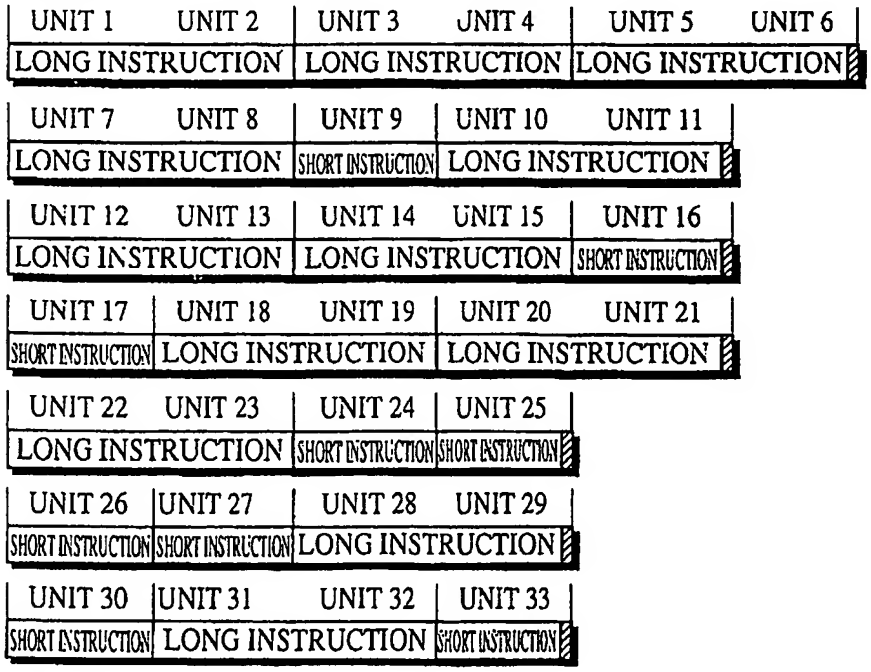


FIG. 2 BACKGROUND ART

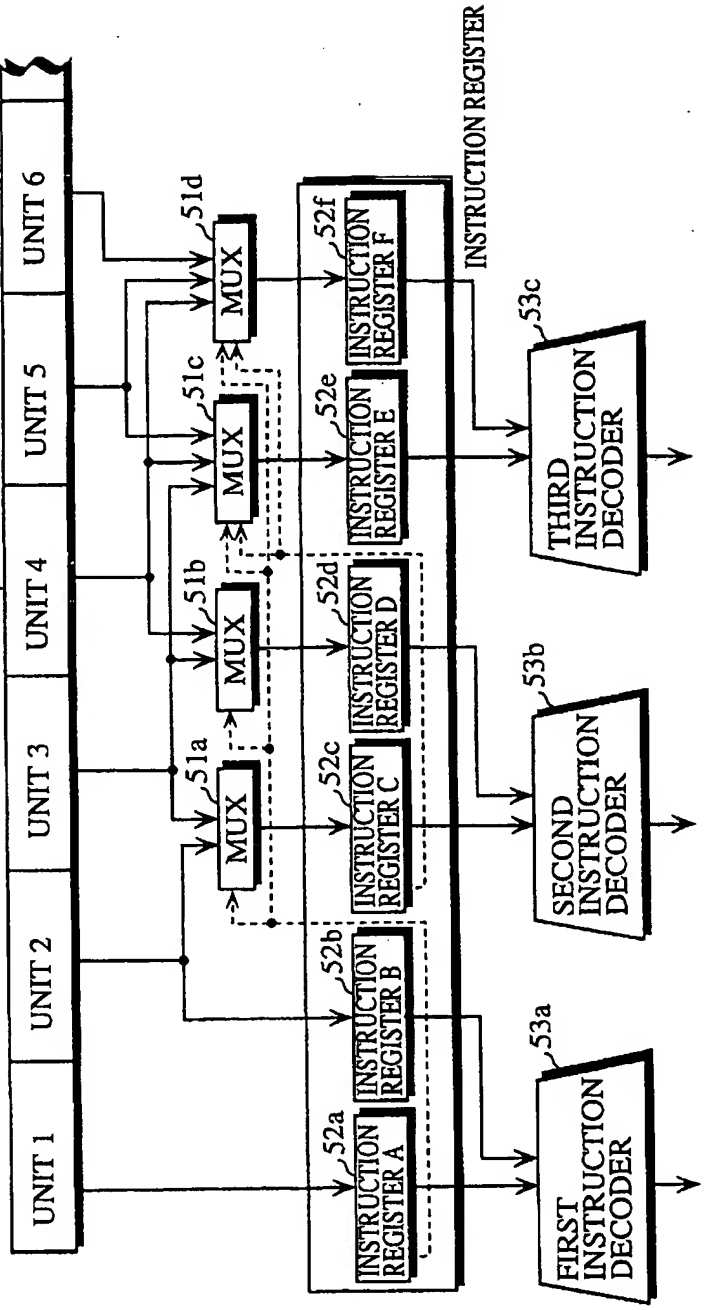


FIG. 3A BACKGROUND ART

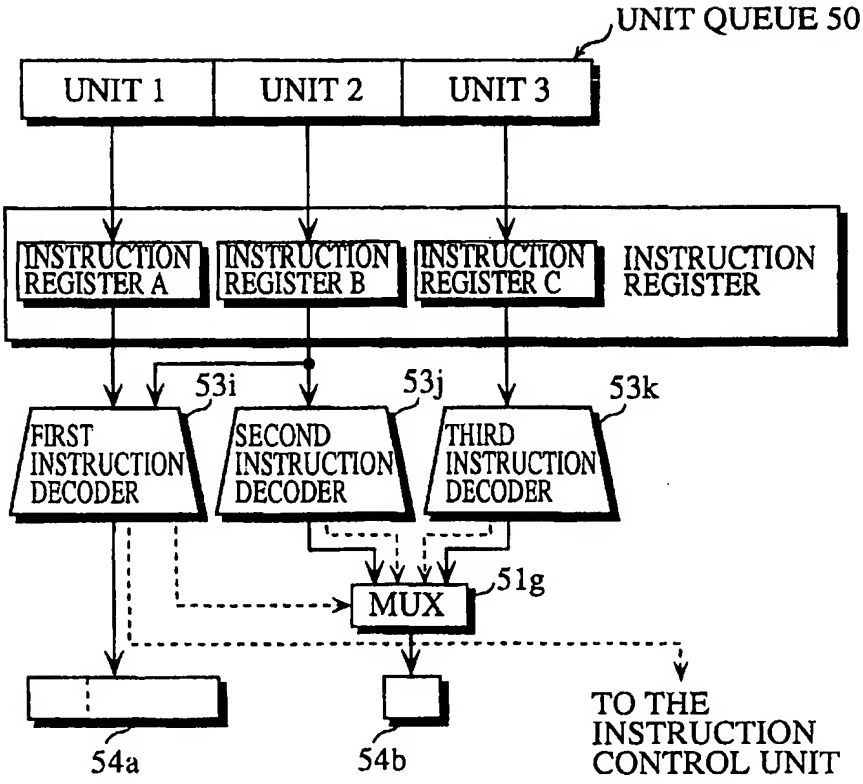


FIG. 3B BACKGROUND ART

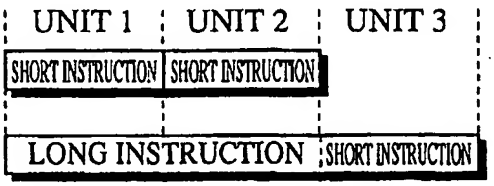


FIG. 4

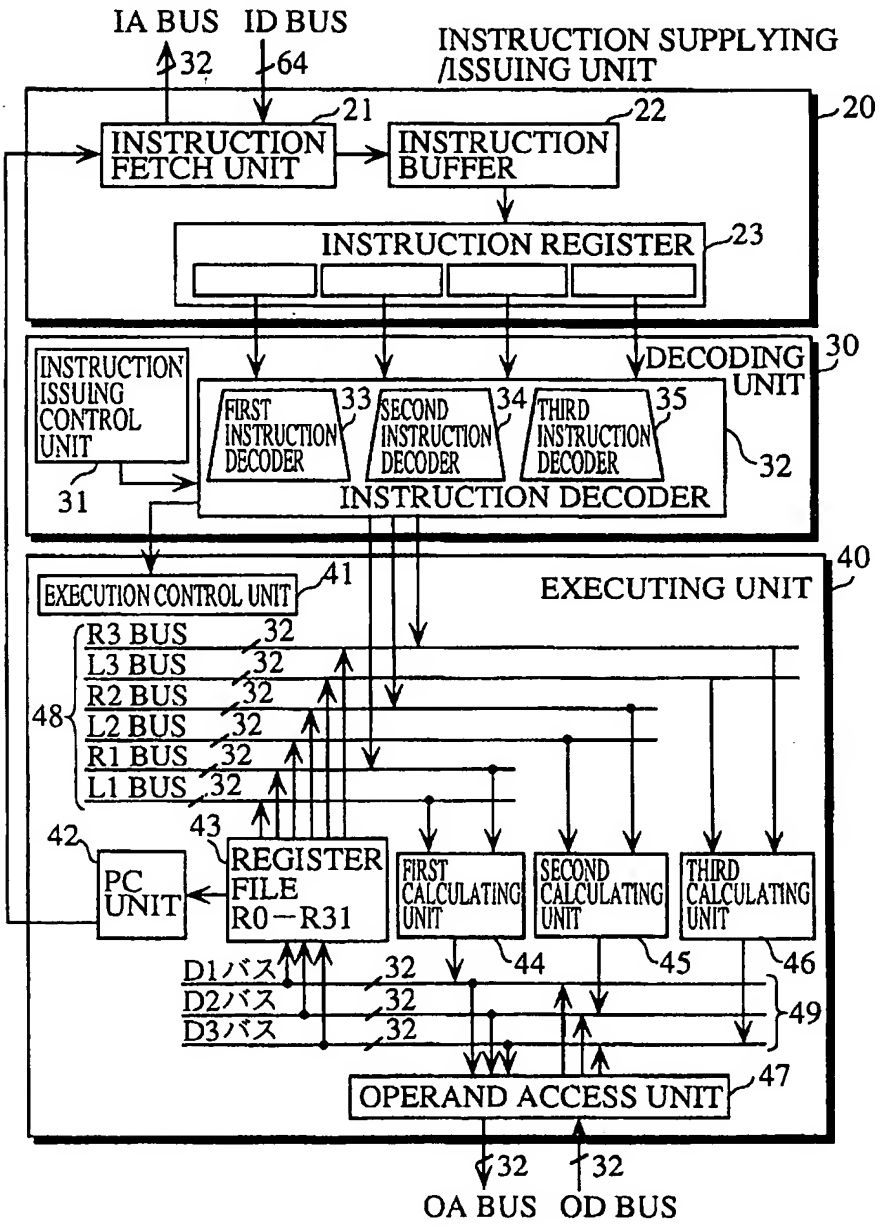

IA BUS
ID BUS
32
64
INSTRUCTION SUPPLYING /ISSUING UNIT
20
21
INSTRUCTION FETCH UNIT
22
INSTRUCTION BUFFER
INSTRUCTION REGISTER
23
DECODING UNIT
30
INSTRUCTION ISSUING CONTROL UNIT
31
FIRST INSTRUCTION DECODER
33
SECOND INSTRUCTION DECODER
34
THIRD INSTRUCTION DECODER
35
INSTRUCTION DECODER
32
EXECUTING UNIT
40
EXECUTION CONTROL UNIT
41
R3 BUS
L3 BUS
R2 BUS
L2 BUS
R1 BUS
L1 BUS
48
43
42
PC UNIT
REGISTER FILE R0－R31
FIRST CALCULATING UNIT
SECOND CALCULATING UNIT
THIRD CALCULATING UNIT
44
45
46
D1バス
D2バス
D3バス
49
OPERAND ACCESS UNIT
47
OA BUS
OD BUS

FIG. 5A

SUPPLYING OF INSTRUCTIONS FROM THE INSTRUCTION FETCH UNIT TO THE INSTRUCTION BUFFER

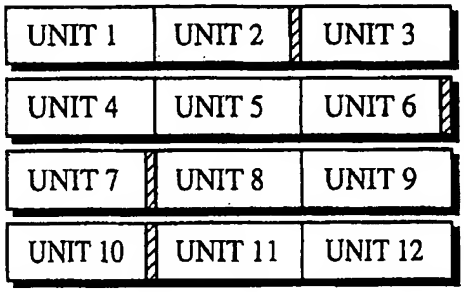


FIG. 5B

SUPPLYING OF INSTRUCTIONS FROM THE INSTRUCTION BUFFER TO THE INSTRUCTION REGISTER

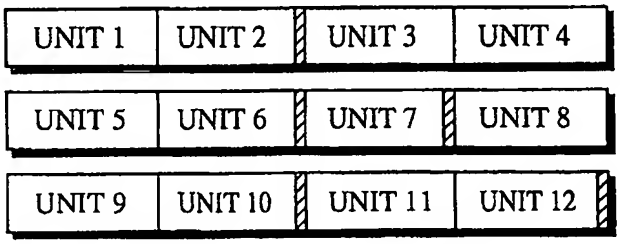
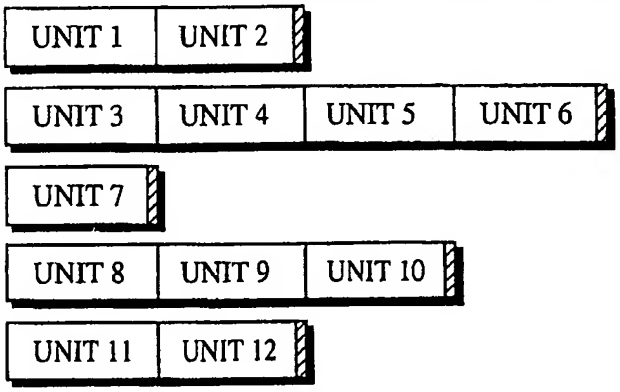


FIG. 5C

ISSUING OF INSTRUCTIONS FROM THE INSTRUCTION REGISTER TO THE INSTRUCTION DECODER (IN UNITS OF PARALLEL EXECUTION CODES)



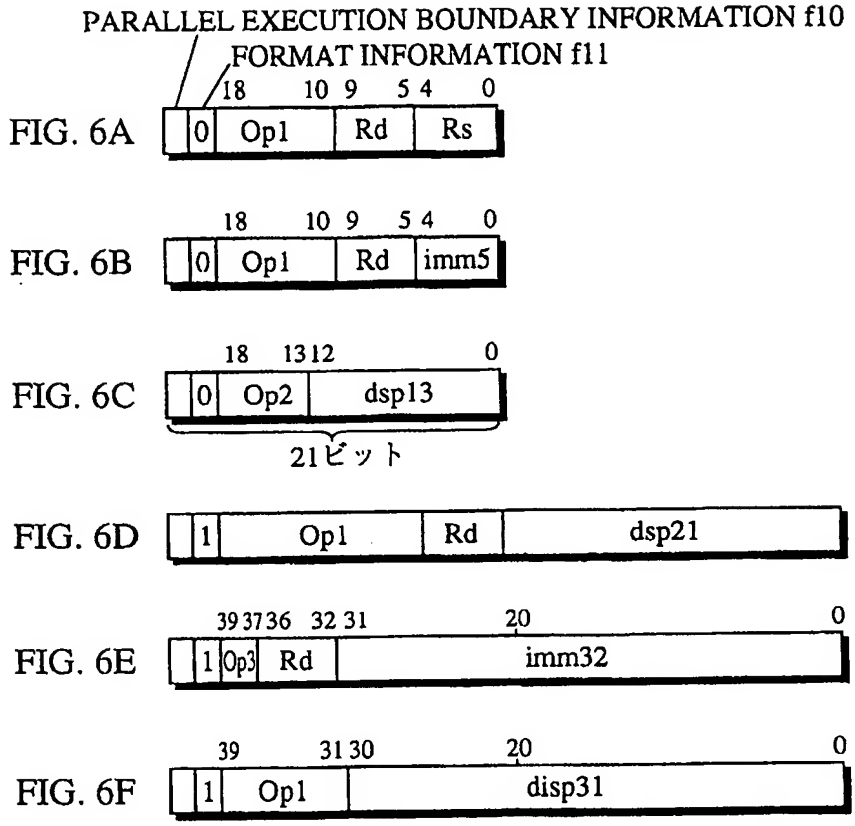
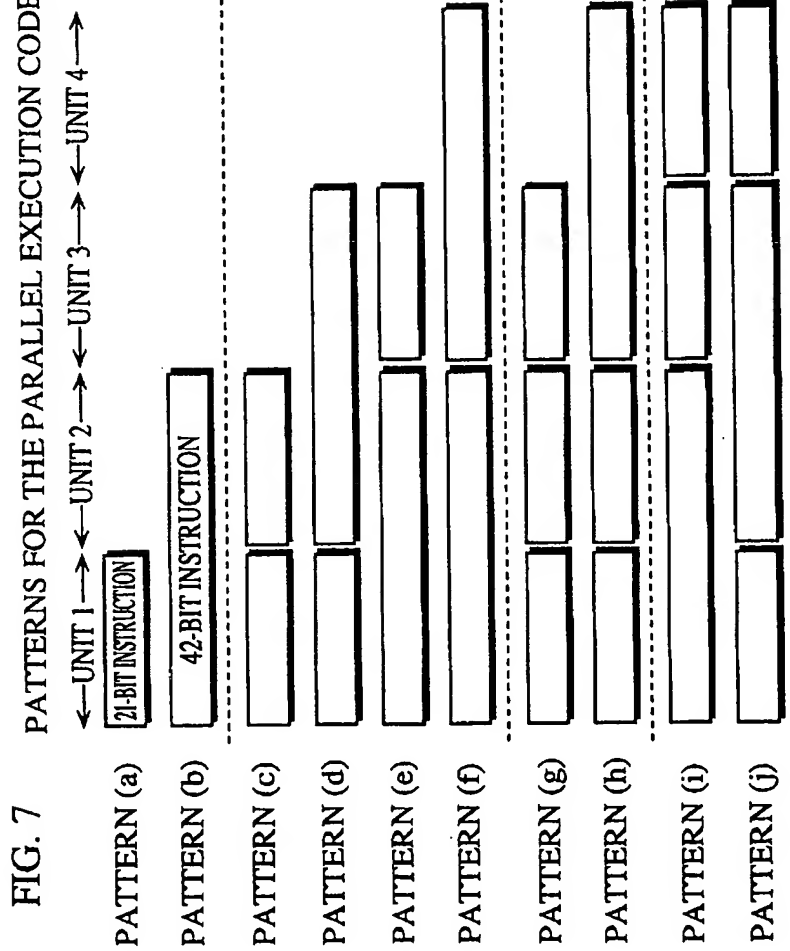

PARALLEL EXECUTION BOUNDARY INFORMATION f10
FORMAT INFORMATION f11
18
10 9
5 4
0
0
Op1
Rd
Rs
FIG. 6A
18
10 9
5 4
0
0
Op1
Rd
imm5
FIG. 6B
18
13 12
0
0
Op2
dsp13
21ビット
FIG. 6C
1
Op1
Rd
dsp21
FIG. 6D
39 37 36
32 31
20
0
1
Op3
Rd
imm32
FIG. 6E
39
31 30
20
0
1
Op1
disp31
FIG. 6F

FIG. 7


PATTERNS FOR THE PARALLEL EXECUTION CODES
←UNIT 1→ ←UNIT 2→ ←UNIT 3→ ←UNIT 4→
21-BIT INSTRUCTION
42-BIT INSTRUCTION
ONE INSTRUCTION EXECUTED
TWO INSTRUCTIONS SIMULTANEOUSLY EXECUTED
THREE INSTRUCTIONS SIMULTANEOUSLY EXECUTED
SIMULTANEOUS ISSUE/EXECUTION IMPOSSIBLE
PATTERN (a)
PATTERN (b)
PATTERN (c)
PATTERN (d)
PATTERN (e)
PATTERN (f)
PATTERN (g)
PATTERN (h)
PATTERN (i)
PATTERN (j)

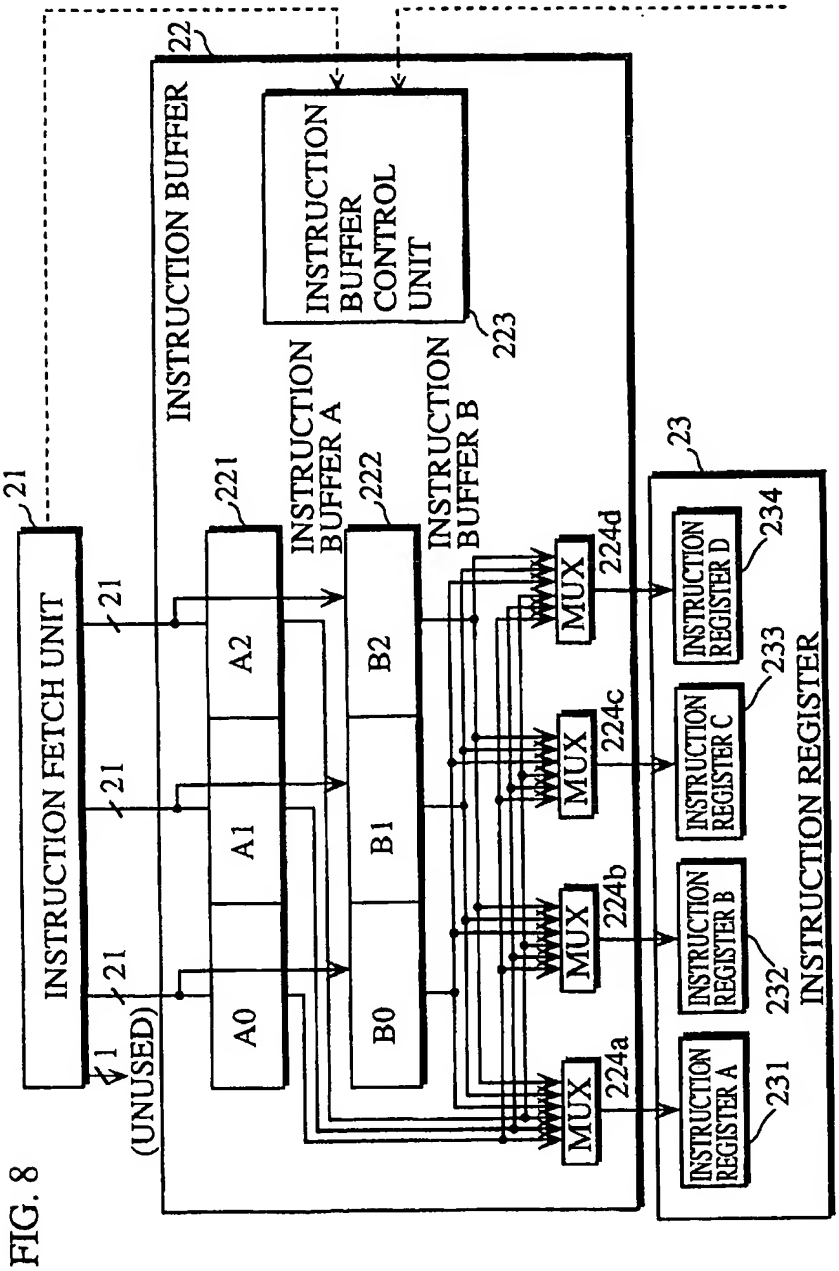

INSTRUCTION FETCH UNIT
21
(UNUSED)
INSTRUCTION BUFFER
22
INSTRUCTION BUFFER CONTROL UNIT
223
INSTRUCTION BUFFER A
221
A0
A1
A2
INSTRUCTION BUFFER B
222
B0
B1
B2
MUX
224a
MUX
224b
MUX
224c
MUX
224d
INSTRUCTION REGISTER
23
INSTRUCTION REGISTER A
231
INSTRUCTION REGISTER B
232
INSTRUCTION REGISTER C
233
INSTRUCTION REGISTER D
234

FIG. 8

FIG. 9A

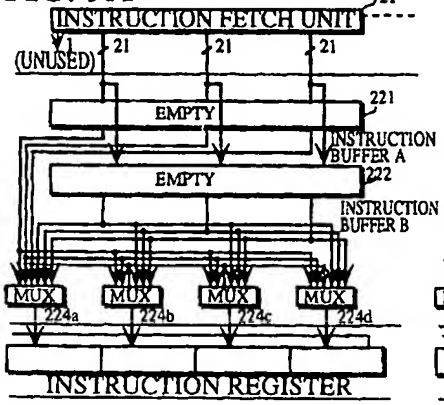


FIG. 9B

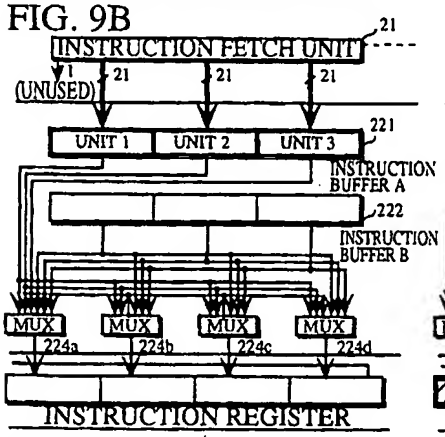


FIG. 9C DISCARDED UNIT

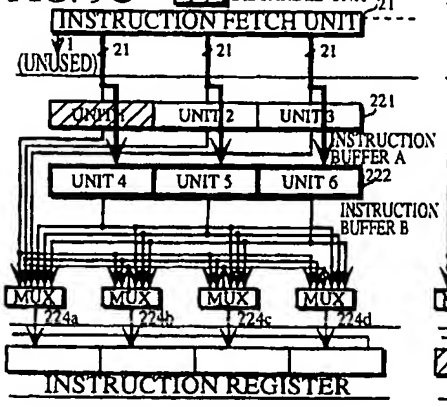


FIG. 9D

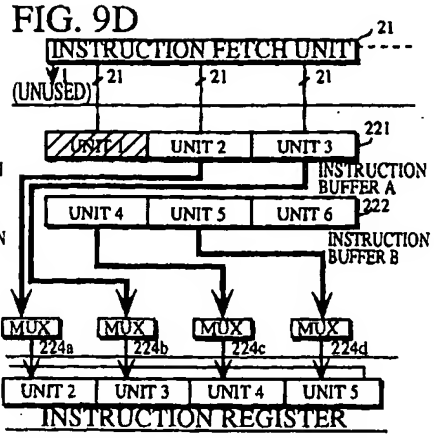


FIG. 9E

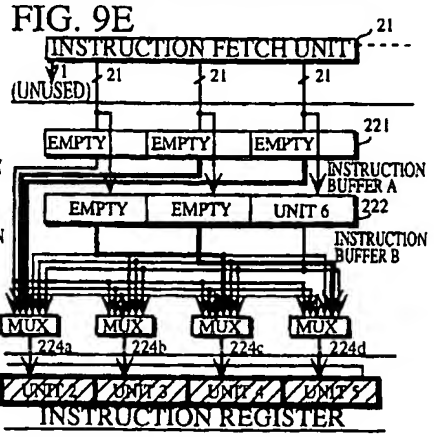


FIG. 9F

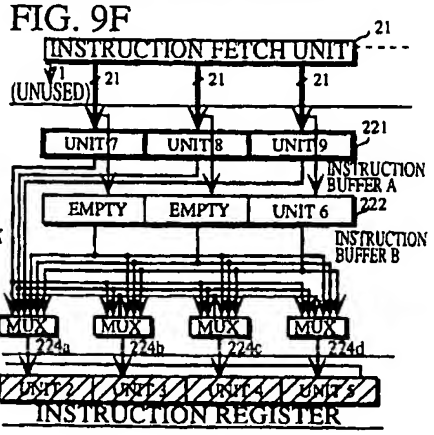


FIG. 10A

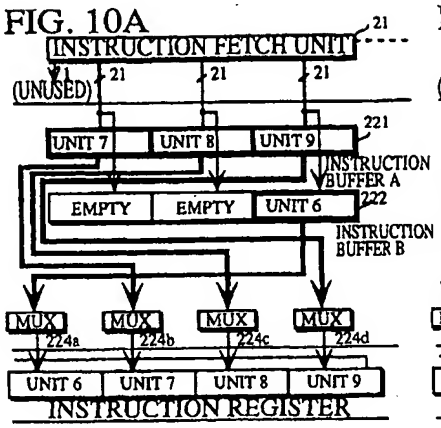


FIG. 10B

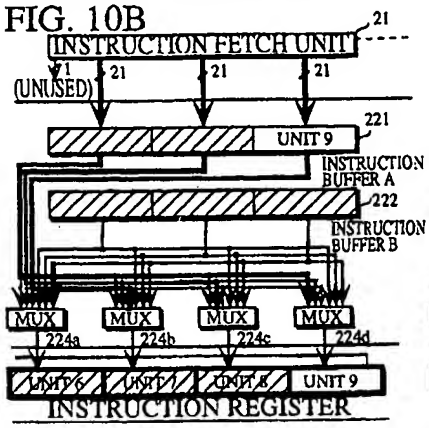


FIG. 10C

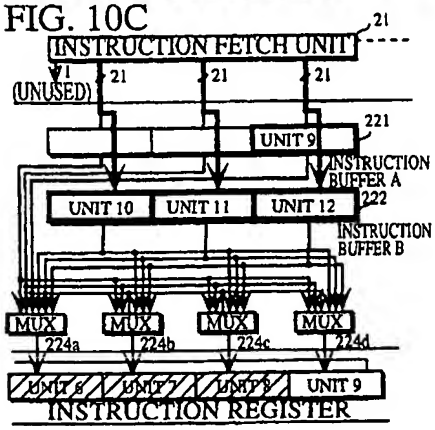


FIG. 10D

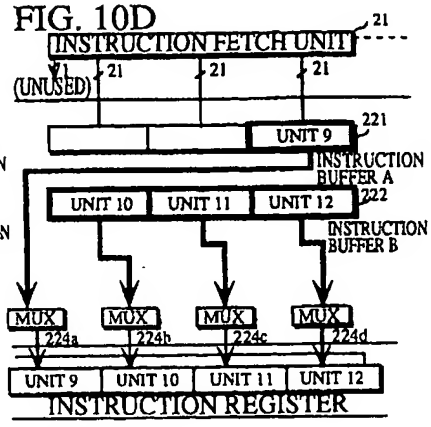
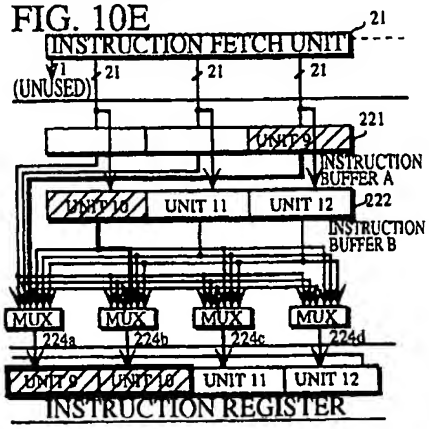


FIG. 10E



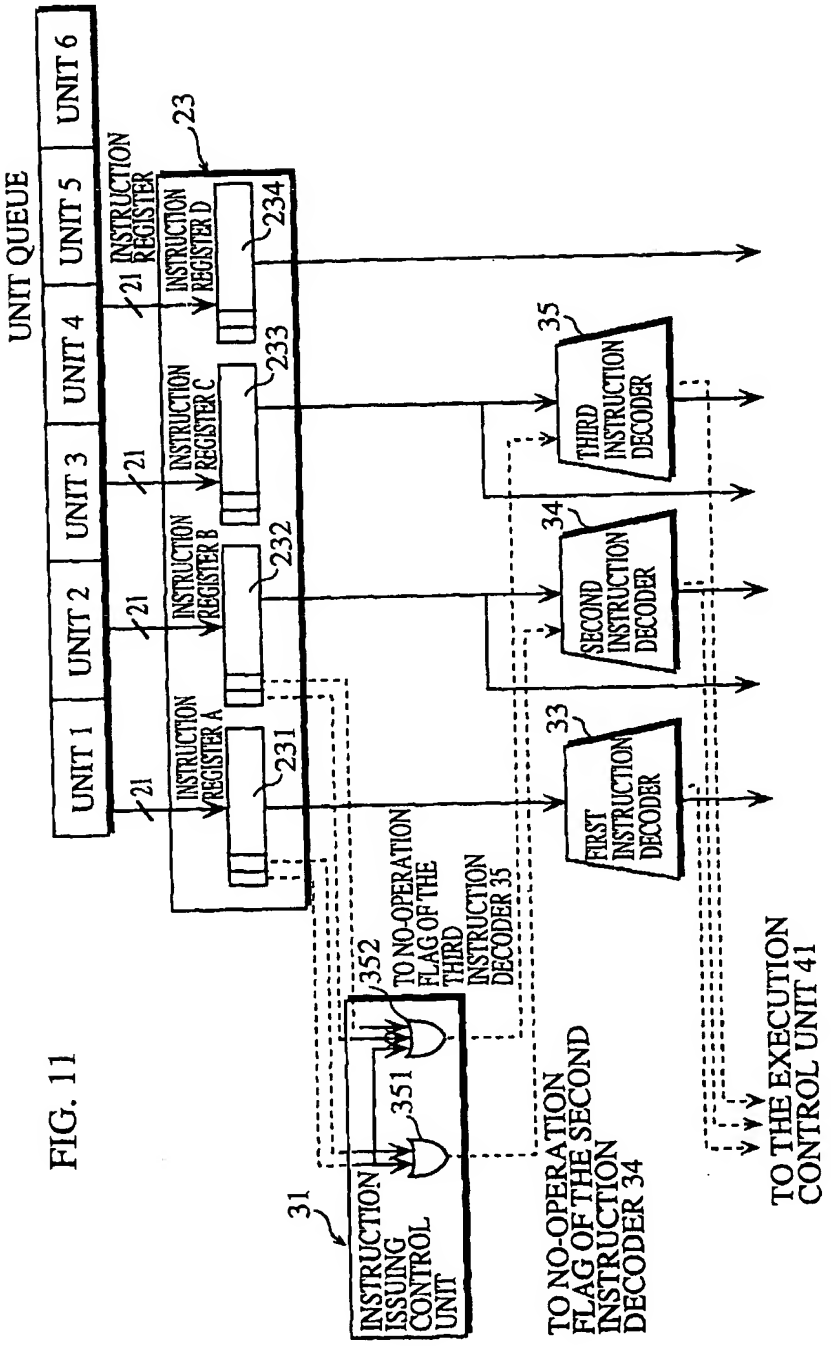

UNIT QUEUE
UNIT 1
UNIT 2
UNIT 3
UNIT 4
UNIT 5
UNIT 6
INSTRUCTION REGISTER
23
21
INSTRUCTION REGISTER A
INSTRUCTION REGISTER B
INSTRUCTION REGISTER C
INSTRUCTION REGISTER D
231
232
233
234
FIRST INSTRUCTION DECODER
SECOND INSTRUCTION DECODER
THIRD INSTRUCTION DECODER
33
34
35
INSTRUCTION ISSUING CONTROL UNIT
31
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34
TO THE EXECUTION CONTROL UNIT 41

FIG. 11

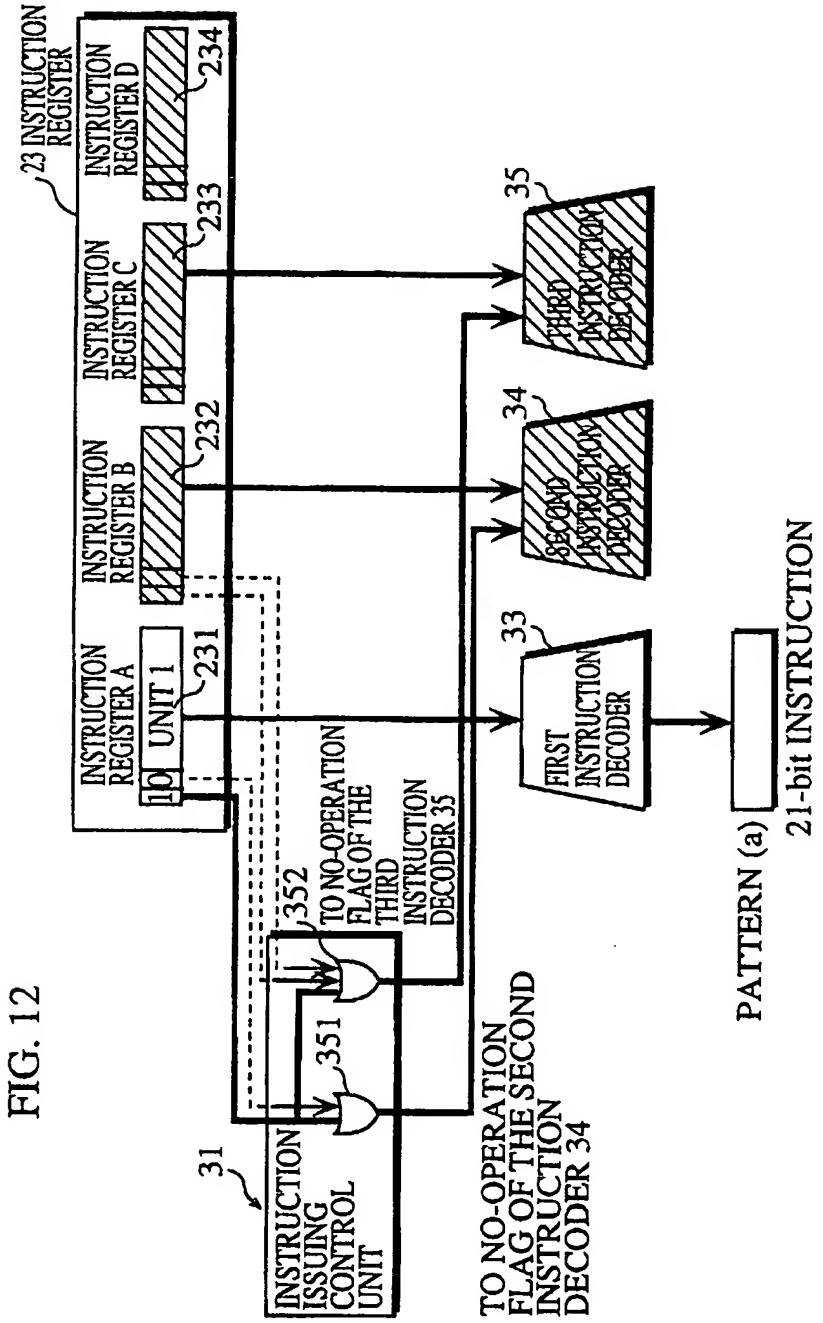

23 INSTRUCTION REGISTER
INSTRUCTION REGISTER A
ID UNIT 1
231
INSTRUCTION REGISTER B
232
INSTRUCTION REGISTER C
233
INSTRUCTION REGISTER D
234
31
INSTRUCTION ISSUING CONTROL UNIT
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34
FIRST INSTRUCTION DECODER
33
SECOND INSTRUCTION DECODER
34
THIRD INSTRUCTION DECODER
35
PATTERN (a)
21-bit INSTRUCTION

FIG. 12

FIG. 13

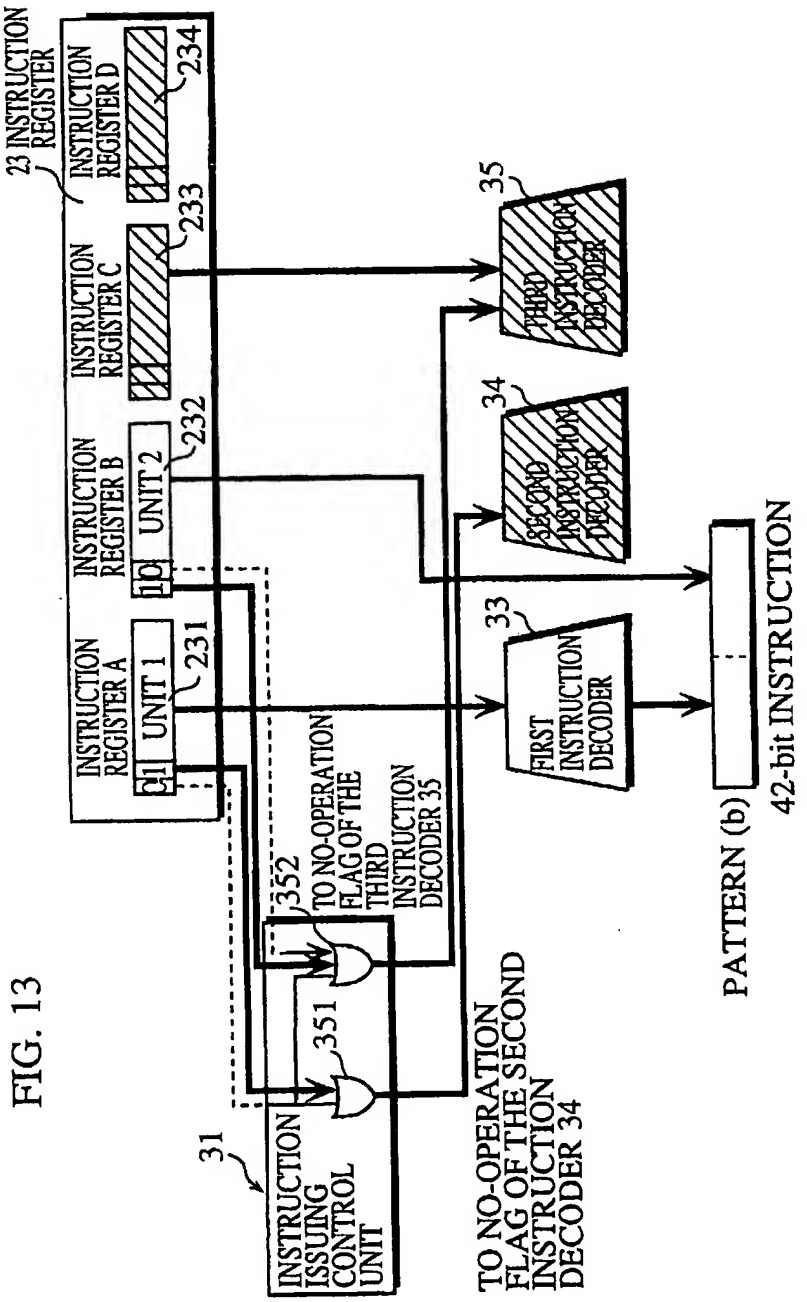

23 INSTRUCTION REGISTER
INSTRUCTION REGISTER A
UNIT 1
231
INSTRUCTION REGISTER B
UNIT 2
232
INSTRUCTION REGISTER C
233
INSTRUCTION REGISTER D
234
31
INSTRUCTION ISSUING CONTROL UNIT
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34
33
FIRST INSTRUCTION DECODER
34
SECOND INSTRUCTION DECODER
35
THIRD INSTRUCTION DECODER
PATTERN (b)
42-bit INSTRUCTION

FIG. 14

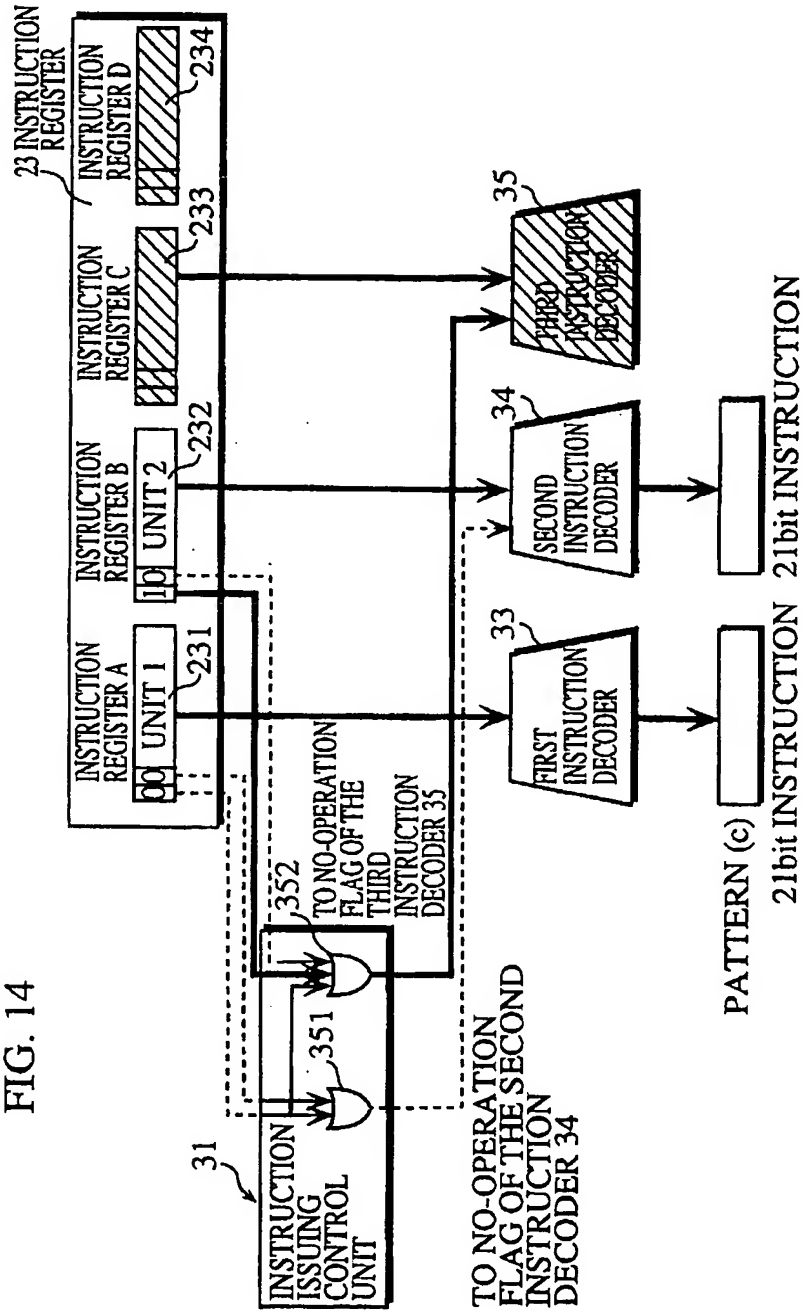

23 INSTRUCTION REGISTER
INSTRUCTION REGISTER A
UNIT 1
231
INSTRUCTION REGISTER B
UNIT 2
232
INSTRUCTION REGISTER C
233
INSTRUCTION REGISTER D
234
31
INSTRUCTION ISSUING CONTROL UNIT
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34
FIRST INSTRUCTION DECODER
33
SECOND INSTRUCTION DECODER
34
THIRD INSTRUCTION DECODER
35
PATTERN (c)
21bit INSTRUCTION
21bit INSTRUCTION

FIG. 15

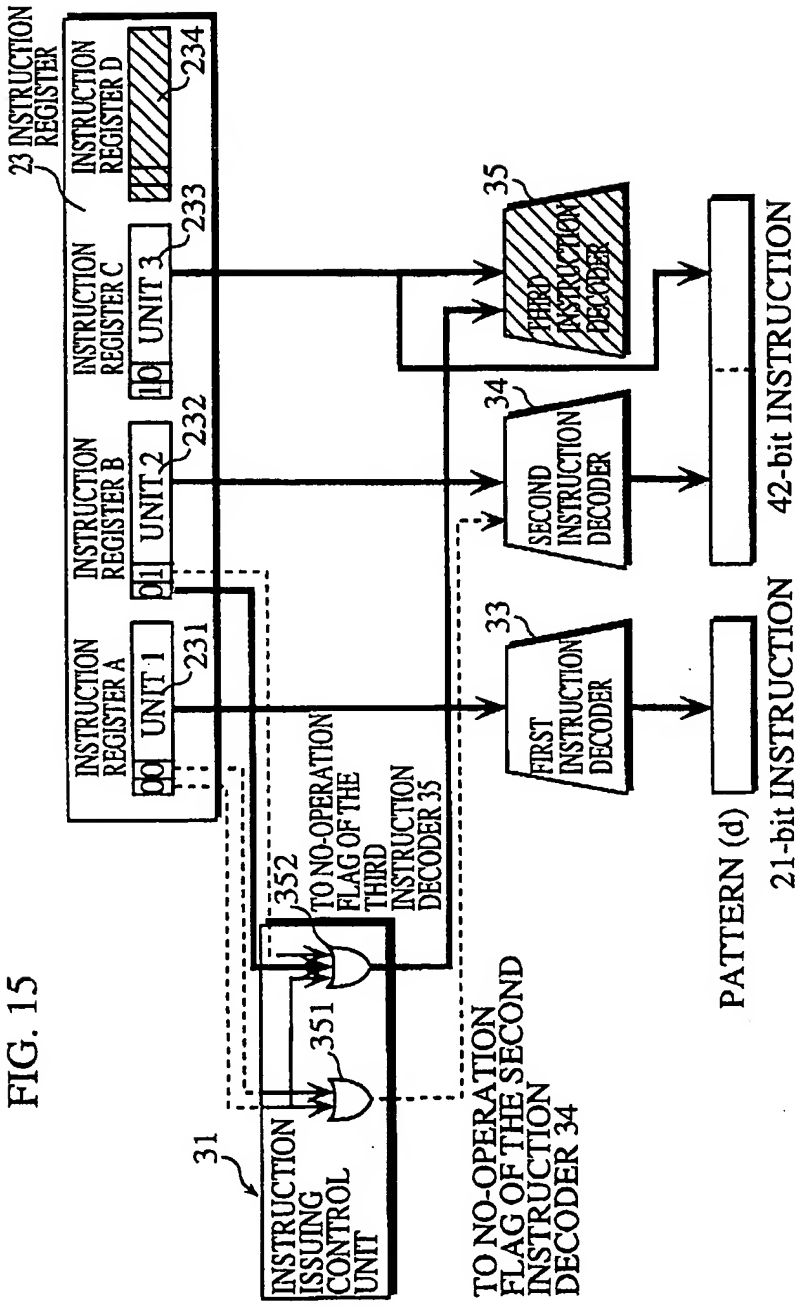
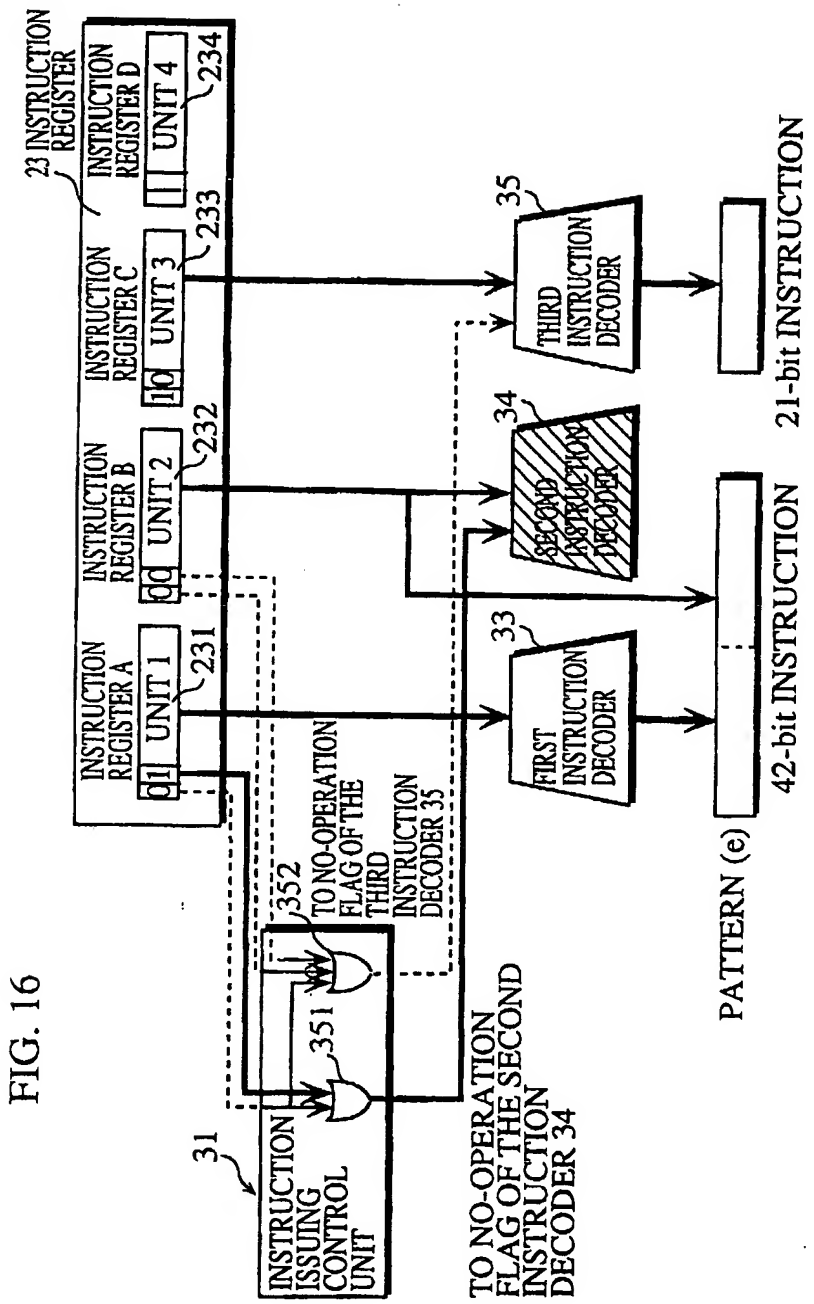

23 INSTRUCTION REGISTER
INSTRUCTION REGISTER A
UNIT 1
231
INSTRUCTION REGISTER B
UNIT 2
232
INSTRUCTION REGISTER C
UNIT 3
233
INSTRUCTION REGISTER D
234
31
INSTRUCTION ISSUING CONTROL UNIT
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34
33
FIRST INSTRUCTION DECODER
34
SECOND INSTRUCTION DECODER
35
THIRD INSTRUCTION DECODER
PATTERN (d)
21-bit INSTRUCTION
42-bit INSTRUCTION

FIG. 16


23 INSTRUCTION REGISTER
INSTRUCTION REGISTER A
UNIT 1
231
INSTRUCTION REGISTER B
UNIT 2
232
INSTRUCTION REGISTER C
UNIT 3
233
INSTRUCTION REGISTER D
UNIT 4
234
31
INSTRUCTION ISSUING CONTROL UNIT
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34
FIRST INSTRUCTION DECODER
33
SECOND INSTRUCTION DECODER
34
THIRD INSTRUCTION DECODER
35
PATTERN (e)
42-bit INSTRUCTION
21-bit INSTRUCTION

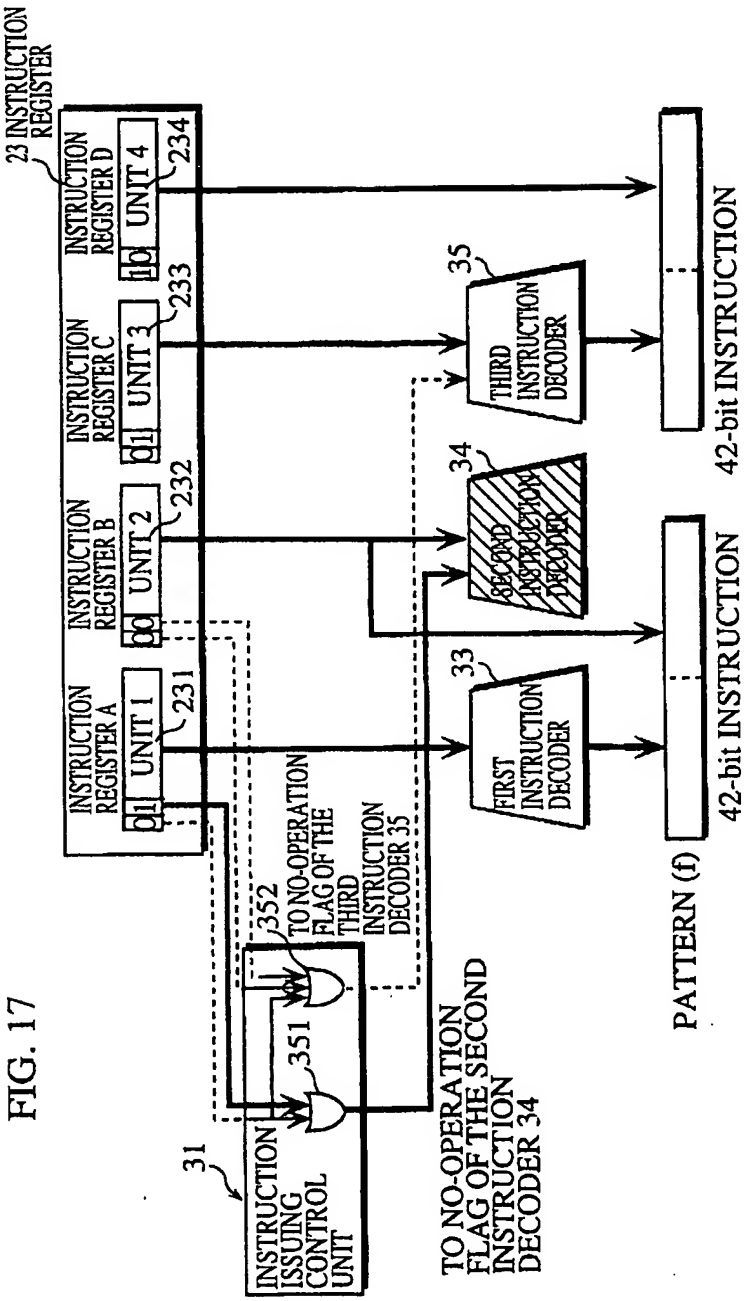

23 INSTRUCTION REGISTER
INSTRUCTION REGISTER A
UNIT 1
231
INSTRUCTION REGISTER B
UNIT 2
232
INSTRUCTION REGISTER C
UNIT 3
233
INSTRUCTION REGISTER D
UNIT 4
234
FIRST INSTRUCTION DECODER
33
SECOND INSTRUCTION DECODER
34
THIRD INSTRUCTION DECODER
35
42-bit INSTRUCTION
42-bit INSTRUCTION
PATTERN (f)
31
INSTRUCTION ISSUING CONTROL UNIT
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34

FIG. 17

FIG. 18

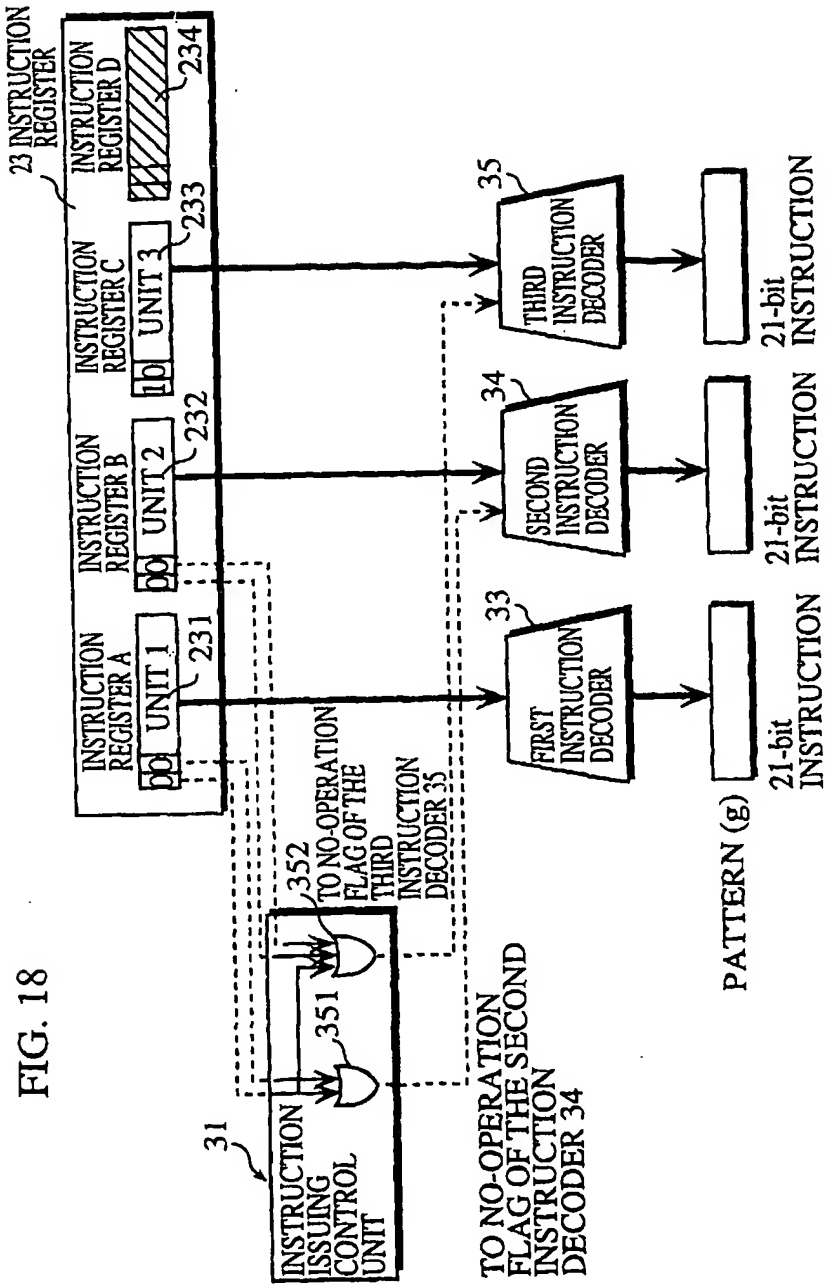

23 INSTRUCTION REGISTER
INSTRUCTION REGISTER A
UNIT 1
231
INSTRUCTION REGISTER B
UNIT 2
232
INSTRUCTION REGISTER C
UNIT 3
233
INSTRUCTION REGISTER D
234
31
INSTRUCTION ISSUING CONTROL UNIT
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34
33
FIRST INSTRUCTION DECODER
34
SECOND INSTRUCTION DECODER
35
THIRD INSTRUCTION DECODER
PATTERN (g)
21-bit INSTRUCTION
21-bit INSTRUCTION
21-bit INSTRUCTION

FIG. 19

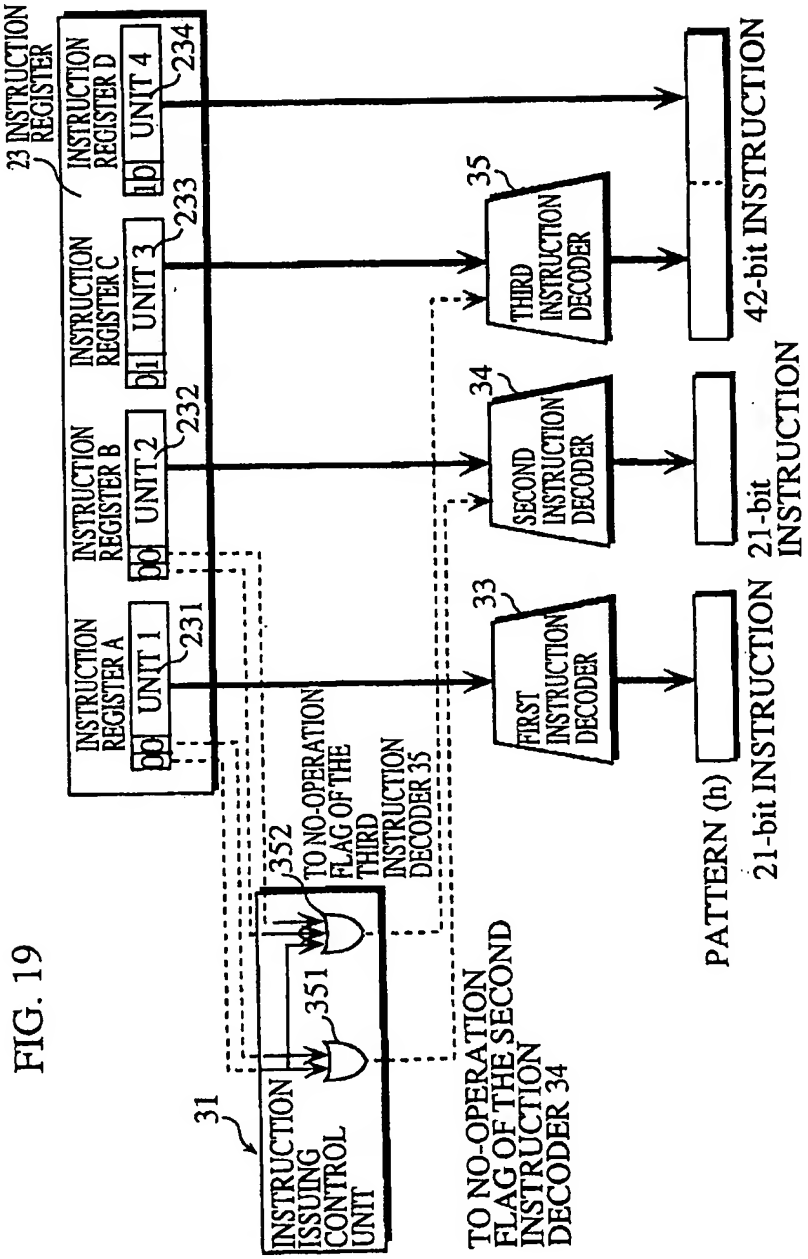

23 INSTRUCTION REGISTER
INSTRUCTION REGISTER A
UNIT 1
231
INSTRUCTION REGISTER B
UNIT 2
232
INSTRUCTION REGISTER C
UNIT 3
233
INSTRUCTION REGISTER D
UNIT 4
234
FIRST INSTRUCTION DECODER
33
SECOND INSTRUCTION DECODER
34
THIRD INSTRUCTION DECODER
35
21-bit INSTRUCTION
42-bit INSTRUCTION
PATTERN (h)
21-bit INSTRUCTION
31
INSTRUCTION ISSUING CONTROL UNIT
351
352
TO NO-OPERATION FLAG OF THE THIRD INSTRUCTION DECODER 35
TO NO-OPERATION FLAG OF THE SECOND INSTRUCTION DECODER 34

FIG. 20

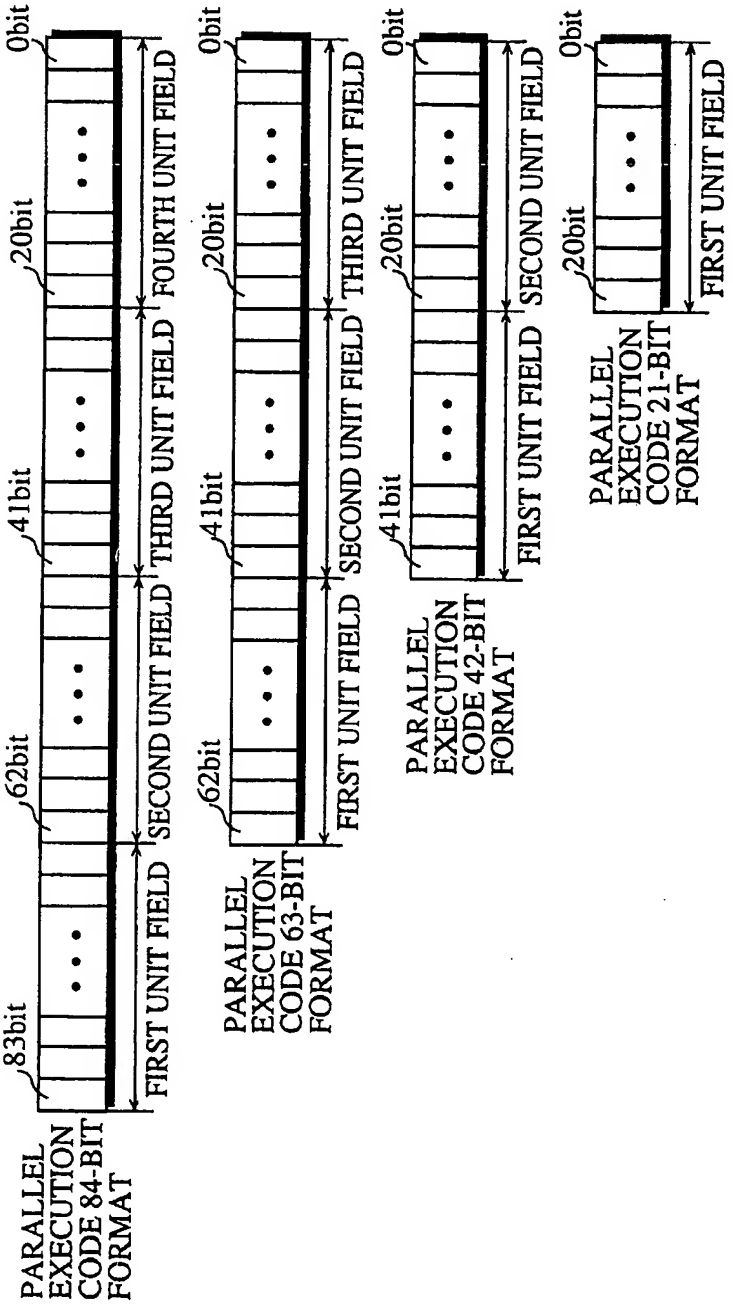

PARALLEL EXECUTION CODE 84-BIT FORMAT
83bit
62bit
41bit
20bit
0bit
FIRST UNIT FIELD
SECOND UNIT FIELD
THIRD UNIT FIELD
FOURTH UNIT FIELD
PARALLEL EXECUTION CODE 63-BIT FORMAT
62bit
41bit
20bit
0bit
FIRST UNIT FIELD
SECOND UNIT FIELD
THIRD UNIT FIELD
PARALLEL EXECUTION CODE 42-BIT FORMAT
41bit
20bit
0bit
FIRST UNIT FIELD
SECOND UNIT FIELD
PARALLEL EXECUTION CODE 21-BIT FORMAT
20bit
0bit
FIRST UNIT FIELD

FIG. 21

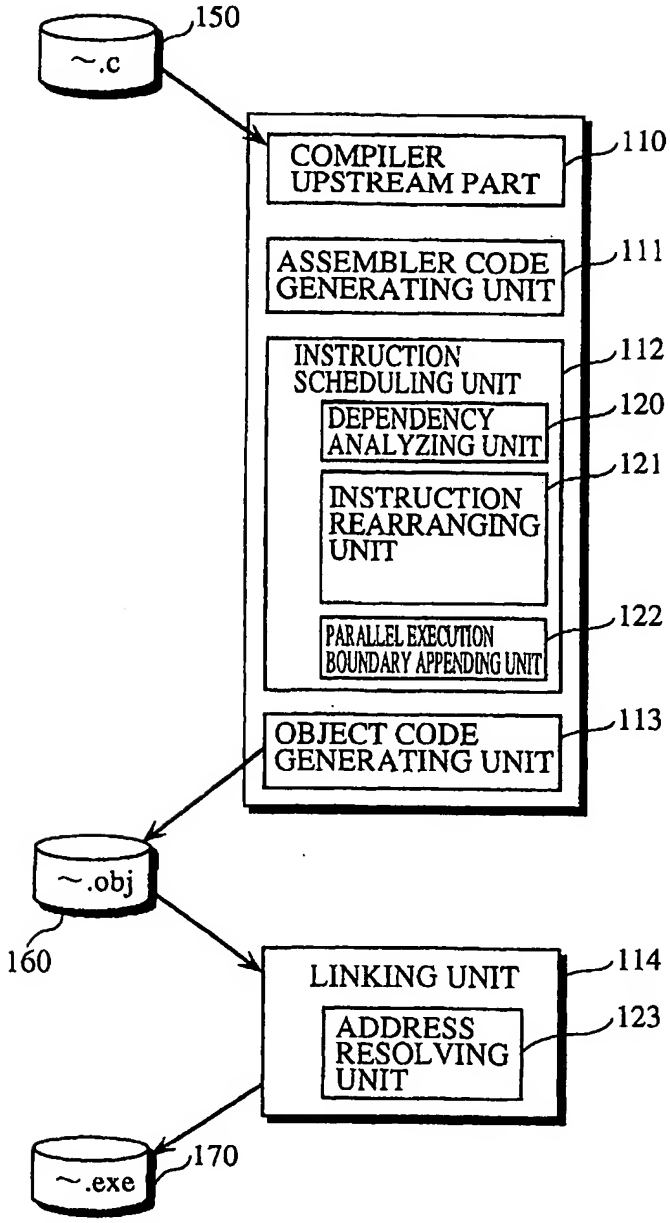

150
~.c
COMPILER UPSTREAM PART
110
ASSEMBLER CODE GENERATING UNIT
111
INSTRUCTION SCHEDULING UNIT
112
DEPENDENCY ANALYZING UNIT
120
INSTRUCTION REARRANGING UNIT
121
PARALLEL EXECUTION BOUNDARY APPENDING UNIT
122
OBJECT CODE GENERATING UNIT
113
~.obj
160
LINKING UNIT
114
ADDRESS RESOLVING UNIT
123
~.exe
170

FIG. 22A

INSTRUCTION 1:ld(mem1),R0
INSTRUCTION 2:add 1,R0
INSTRUCTION 3:st R0,(mem2)
INSTRUCTION 4:mov R1,R0
INSTRUCTION 5:mov R2,R3
INSTRUCTION 6:add R3,R0
INSTRUCTION 7:st R0,(mem3)

FIG. 22B

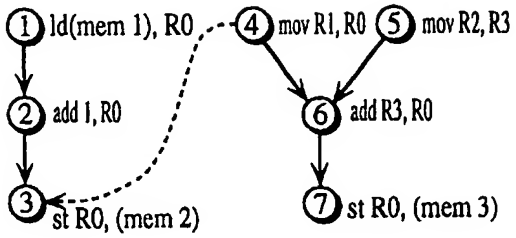


FIG. 22C

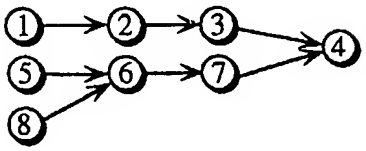


FIG. 22D

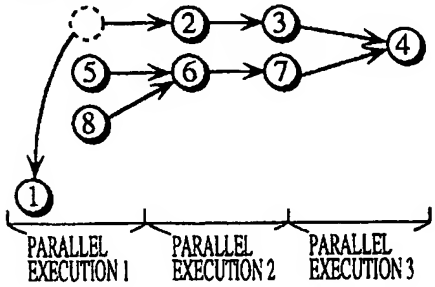


FIG. 22E

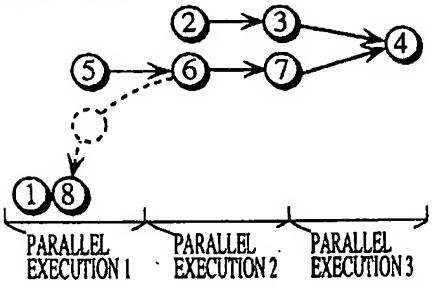


FIG. 22F

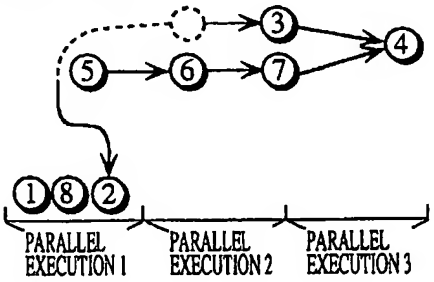


FIG. 23A

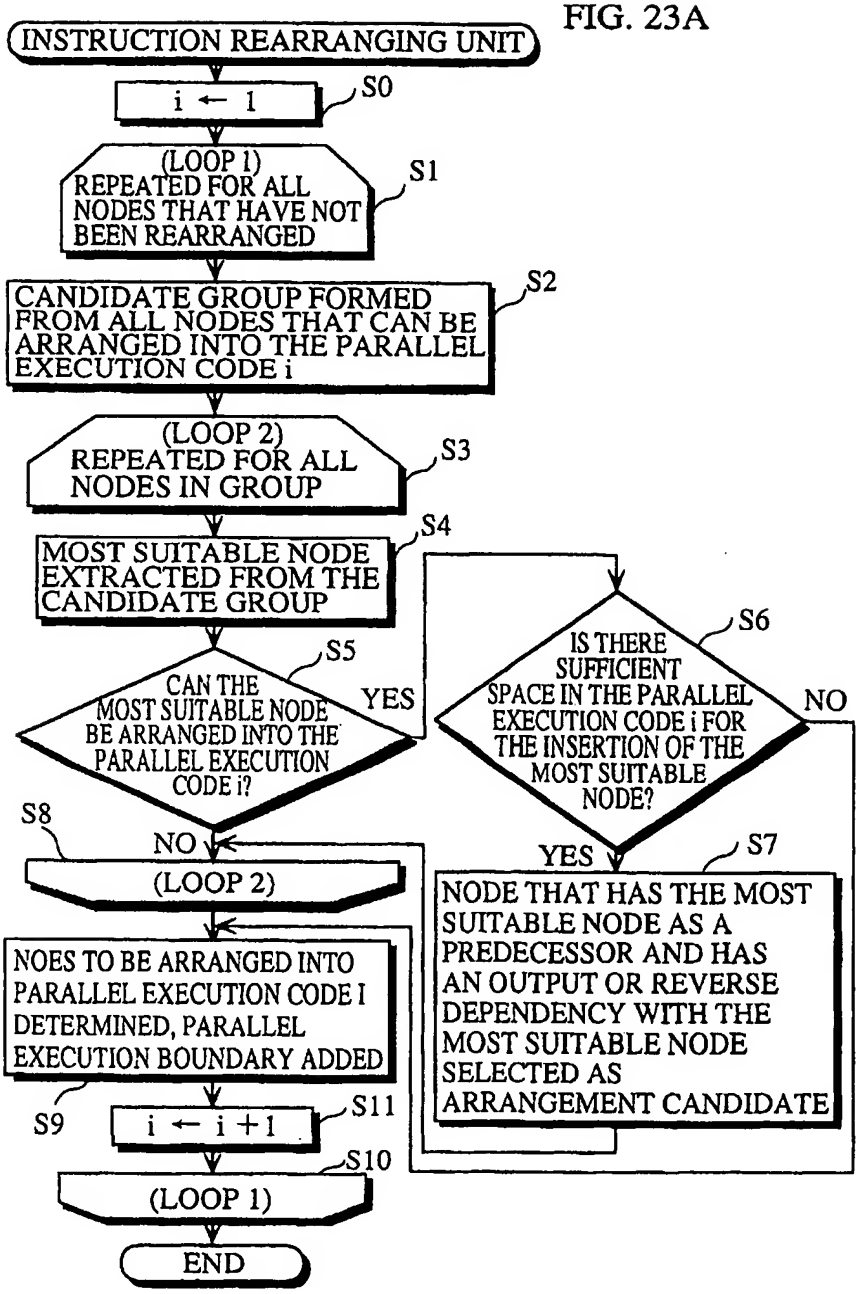

INSTRUCTION REARRANGING UNIT
i ← 1
S0
(LOOP 1)
REPEATED FOR ALL NODES THAT HAVE NOT BEEN REARRANGED
S1
CANDIDATE GROUP FORMED FROM ALL NODES THAT CAN BE ARRANGED INTO THE PARALLEL EXECUTION CODE i
S2
(LOOP 2)
REPEATED FOR ALL NODES IN GROUP
S3
MOST SUITABLE NODE EXTRACTED FROM THE CANDIDATE GROUP
S4
CAN THE MOST SUITABLE NODE BE ARRANGED INTO THE PARALLEL EXECUTION CODE i?
S5
YES
IS THERE SUFFICIENT SPACE IN THE PARALLEL EXECUTION CODE i FOR THE INSERTION OF THE MOST SUITABLE NODE?
S6
NO
YES
S7
NODE THAT HAS THE MOST SUITABLE NODE AS A PREDECESSOR AND HAS AN OUTPUT OR REVERSE DEPENDENCY WITH THE MOST SUITABLE NODE SELECTED AS ARRANGEMENT CANDIDATE
S8
NO
(LOOP 2)
NOES TO BE ARRANGED INTO PARALLEL EXECUTION CODE I DETERMINED, PARALLEL EXECUTION BOUNDARY ADDED
S9
i ← i + 1
S11
S10
(LOOP 1)
END

FIG. 23B

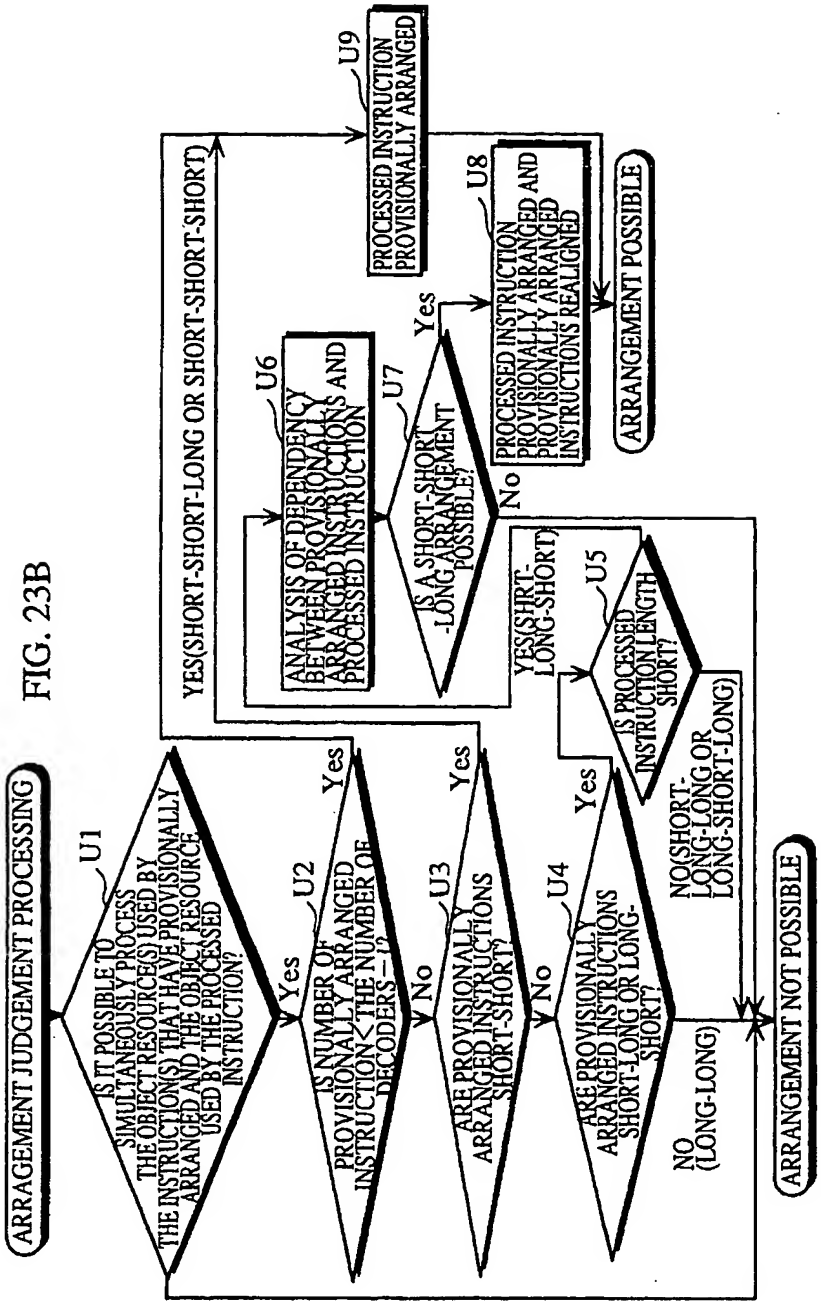
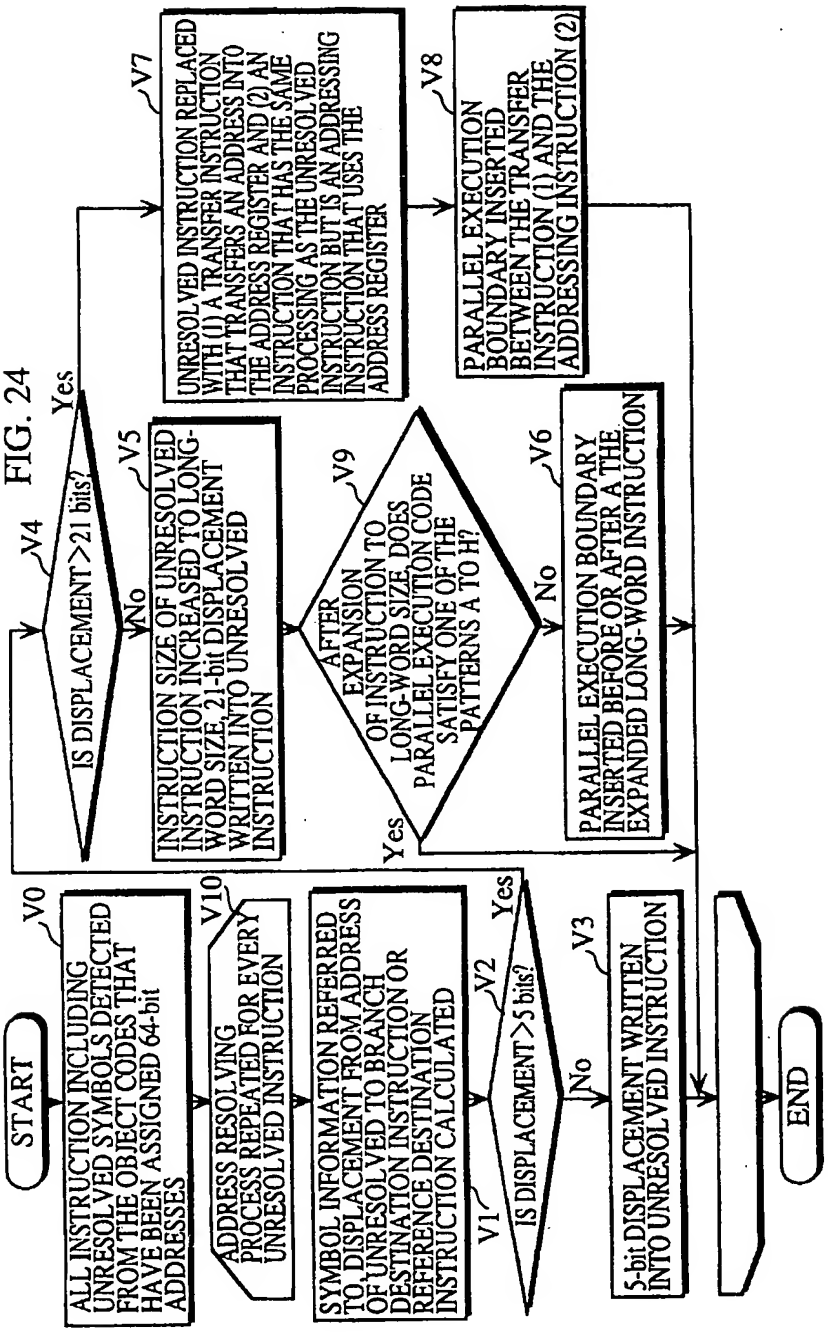

ARRAGEMENT JUDGEMENT PROCESSING
U1
IS IT POSSIBLE TO SIMULTANEOUSLY PROCESS THE OBJECT RESOURCE(S) USED BY THE INSTRUCTION(S) THAT HAVE PROVISIONALLY ARRANGED AND THE OBJECT RESOURCE USED BY THE PROCESSED INSTRUCTION?
Yes
U2
IS NUMBER OF PROVISIONALLY ARRANGED INSTRUCTION < THE NUMBER OF DECODERS - 1?
Yes
No
U3
ARE PROVISIONALLY ARRANGED INSTRUCTIONS SHORT-SHORT?
Yes
No
U4
ARE PROVISIONALLY ARRANGED INSTRUCTIONS SHORT-LONG OR LONG-SHORT?
Yes
NO (LONG-LONG)
U5
IS PROCESSED INSTRUCTION LENGTH SHORT?
YES(SHORT-LONG-SHORT)
NO(SHORT-LONG-LONG OR LONG-SHORT-LONG)
YES(SHORT-SHORT-LONG OR SHORT-SHORT-SHORT)
U6
ANALYSIS OF DEPENDENCY BETWEEN PROVISIONALLY ARRANGED INSTRUCTIONS AND PROCESSED INSTRUCTION
U7
IS A SHORT-SHORT-LONG ARRANGEMENT POSSIBLE?
Yes
No
U8
PROCESSED INSTRUCTION PROVISIONALLY ARRANGED AND PROVISIONALLY ARRANGED INSTRUCTIONS REALIGNED
U9
PROCESSED INSTRUCTION PROVISIONALLY ARRANGED
ARRANGEMENT POSSIBLE
ARRANGEMENT NOT POSSIBLE

FIG. 24


START
V0
ALL INSTRUCTION INCLUDING UNRESOLVED SYMBOLS DETECTED FROM THE OBJECT CODES THAT HAVE BEEN ASSIGNED 64-bit ADDRESSES
V10
ADDRESS RESOLVING PROCESS REPEATED FOR EVERY UNRESOLVED INSTRUCTION
SYMBOL INFORMATION REFERRED TO, DISPLACEMENT FROM ADDRESS OF UNRESOLVED TO BRANCH DESTINATION INSTRUCTION OR REFERENCE DESTINATION INSTRUCTION CALCULATED
V1
V2
IS DISPLACEMENT>5 bits?
Yes
No
V3
5-bit DISPLACEMENT WRITTEN INTO UNRESOLVED INSTRUCTION
END
V4
IS DISPLACEMENT>21 bits?
Yes
No
V5
INSTRUCTION SIZE OF UNRESOLVED INSTRUCTION INCREASED TO LONG-WORD SIZE, 21-bit DISPLACEMENT WRITTEN INTO UNRESOLVED INSTRUCTION
V7
UNRESOLVED INSTRUCTION REPLACED WITH (1) A TRANSFER INSTRUCTION THAT TRANSFERS AN ADDRESS INTO THE ADDRESS REGISTER AND (2) AN INSTRUCTION THAT HAS THE SAME PROCESSING AS THE UNRESOLVED INSTRUCTION BUT IS AN ADDRESSING INSTRUCTION THAT USES THE ADDRESS REGISTER
V8
PARALLEL EXECUTION BOUNDARY INSERTED BETWEEN THE TRANSFER INSTRUCTION (1) AND THE ADDRESSING INSTRUCTION (2)
V9
AFTER EXPANSION OF INSTRUCTION TO LONG-WORD SIZE, DOES PARALLEL EXECUTION CODE SATISFY ONE OF THE PATTERNS A TO H?
Yes
No
V6
PARALLEL EXECUTION BOUNDARY INSERTED BEFORE OR AFTER A THE EXPANDED LONG-WORD INSTRUCTION

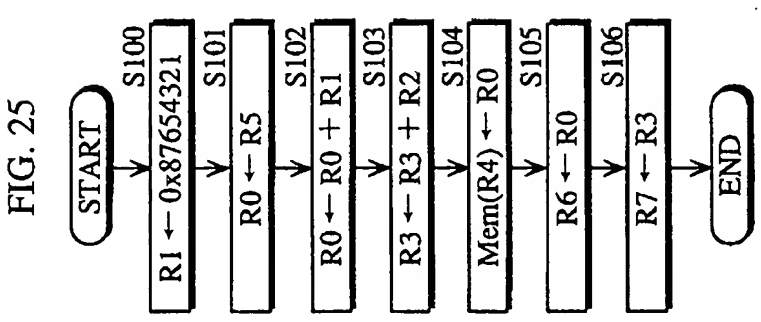


FIG. 25

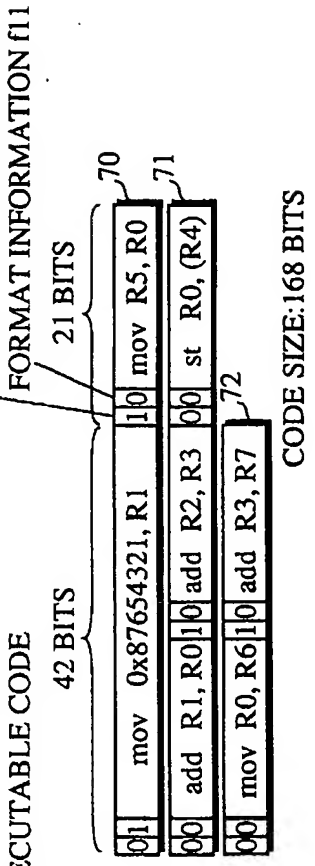


FIG. 26A

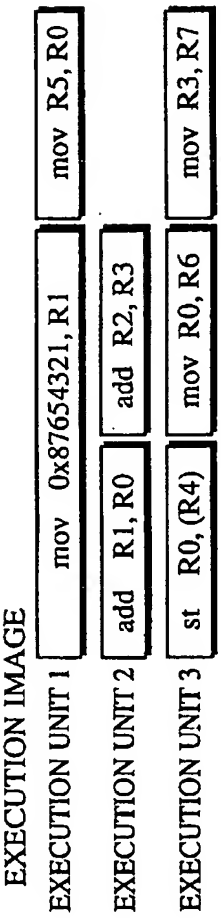


FIG. 26B

FIG. 27A

INSTRUCTION 1	mov 0x0100, R0
INSTRUCTION 2	st R0, (SP)
INSTRUCTION 3	mov R1, R2
INSTRUCTION 4	mov R3, R4
INSTRUCTION 5	add R2, R4

FIG. 27B

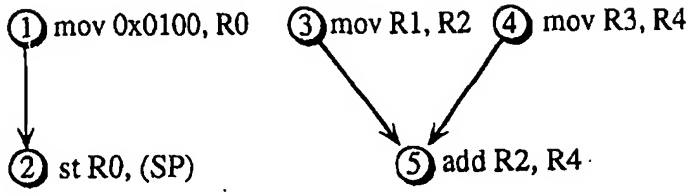


FIG. 27C

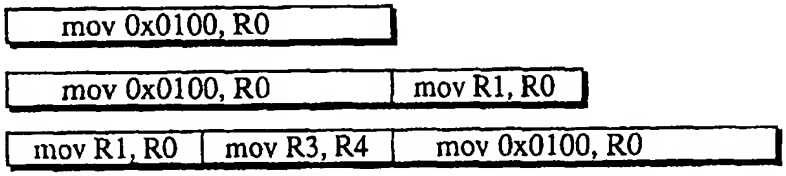


FIG. 27D

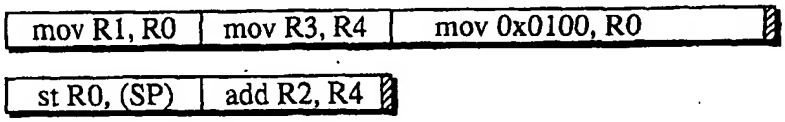


FIG. 27E

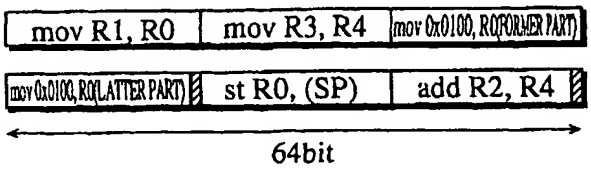


FIG. 28A

INSTRUCTION 6	ld (mem 1), R0
INSTRUCTION 7	st R0, (SP)
INSTRUCTION 8	mov R1, R2
INSTRUCTION 9	mov R3, R4
INSTRUCTION 10	add R2, R4

FIG. 28B

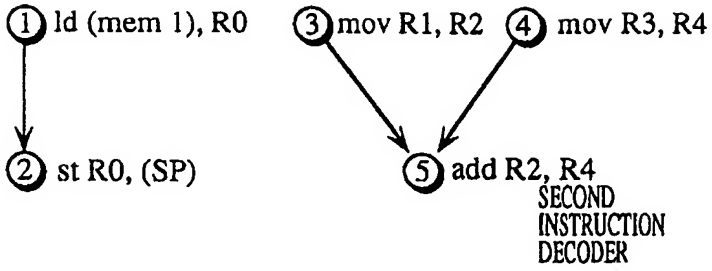


FIG. 28C

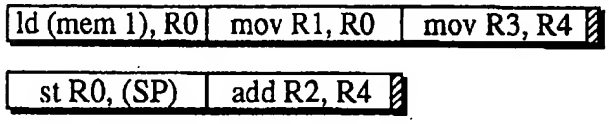


FIG. 28D

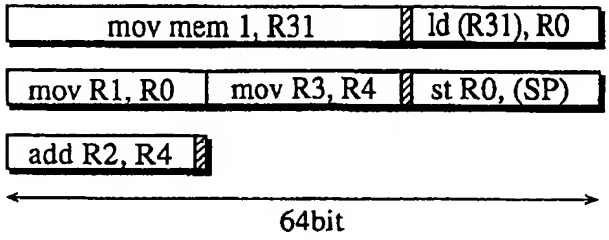


FIG. 29A

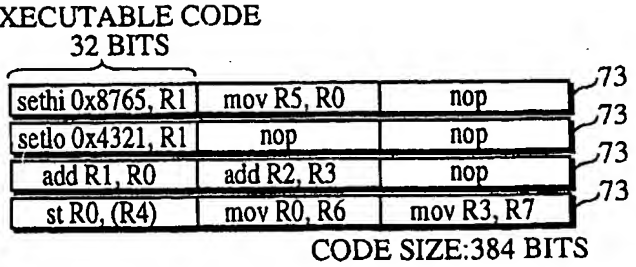


FIG. 29B

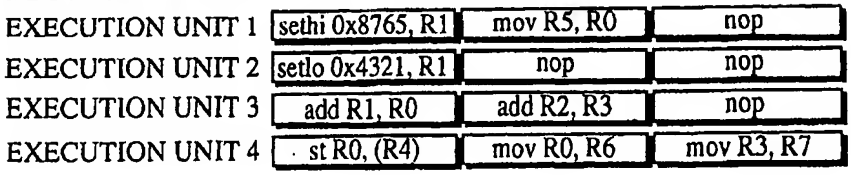


FIG. 30A

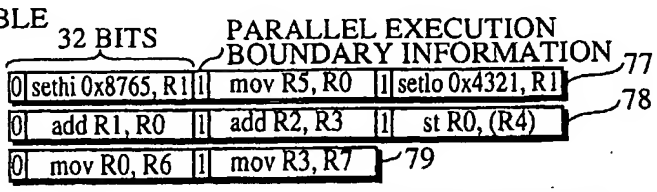


FIG. 30B

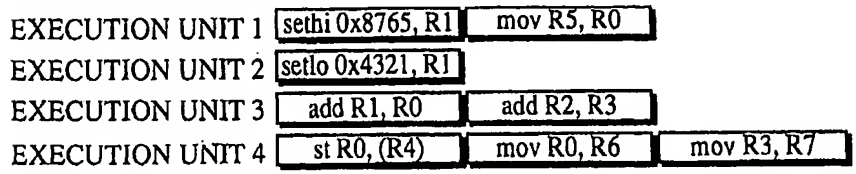


FIG. 31A

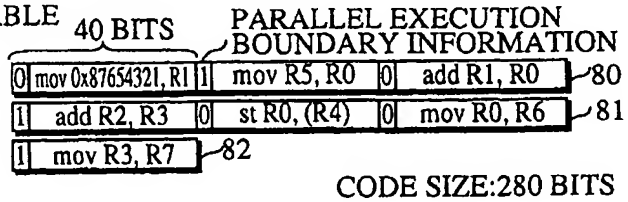


FIG. 31B